MTC-20146

ADSL
DMT Transceiver
with ATM Framer and
integrated controller
Preliminary Information

Data Sheet

Rev. 1.0 - January 1999

Features

- DMT modem and embedded controller, ATM framer
- Supports ANSI TI.413 issue 2, ITU G.992.1, and G.992.2 standards
- Power consumption 1.3 Watt at 3.3V
- Standard Utopia level 1 and level 2 ATM interfaces
- Parallel or serial modem control interface (CTRLE) for glueless connection to management entities
- Supports code download
- External Bus Interface for 16-bit SDRAM
- Packages
  176 TQFP Package
  208 DQFP Package

General Description

The MTC-20146 is the DMT modem, ATM Framer and controller chip of the MTK-20140 Rate adaptive ADSL DynaMiTe chipset.
When used in conjunction with the MTC-20144 analog front-end, the product supports ANSI TI.413 release 2 ADSL specification and is SW upgradeable to ITU G.992.1 and G.992.2 (G.Lite). The MTC-20146 may be used in both central office (ATU-C) and remote (ATU-R) applications. It provides both a cell based UTOPIA Level 1 and 2 ATM data interface.

Ordering Information

Part number	Package	Temp
MTC-20146TQ-I	176 pin TQFP	-40 + 85°C
MTC-20146TQ-C	176 pin TQFP	0 + 70°C
MTC-20146DQ-i	208 pin DQFP	-40 + 85°C
MTC-20146DQ-C	208 pin DQFP	0 + 70°C

Can also be ordered using kit number MTK-20140

ALCATEL

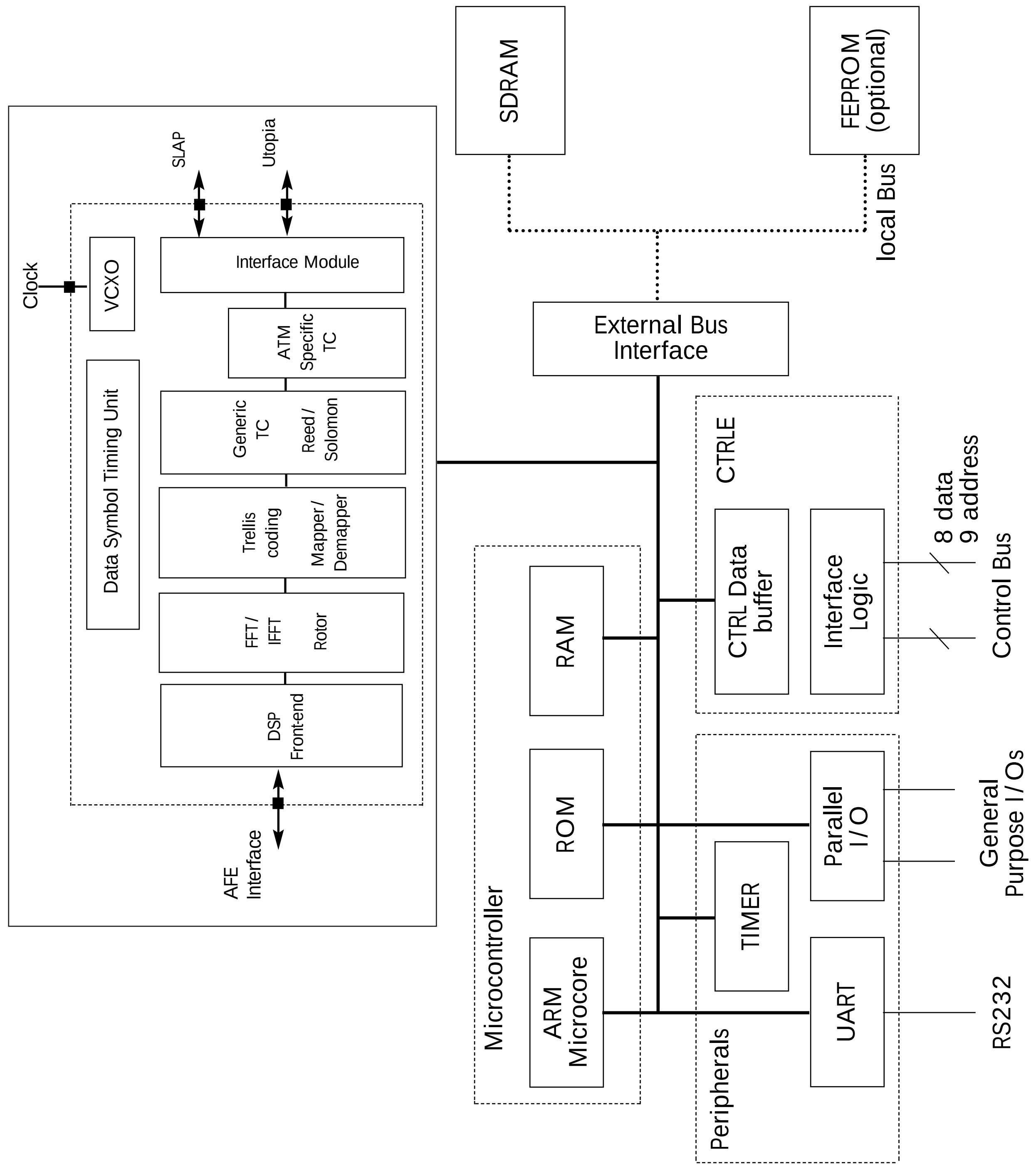

Fig.1: MTC-20146 Block diagram

Functional Description

Figure 1 shows the global block diagram of the MTC-20146.
The functions can be grouped into the following:
- Microcontroller
- External Bus Interface
- Control Interface (CTRLE)
- DMT modem
- AFE interface
- Utopia interface
- Peripherals
- Miscellaneous

Microcontroller

The microcontroller block includes an ARM-based microcore and its associated internal memory. 16 Kbytes on internal RAM and 128 x 32-bit words of ROM are foreseen. The ROM essentially contains the boot sequence needed for code download at startup. The use of the ROM by the microcore is defined by the state of the TROM pin during reset.

External Bus Interface

The External Bus Interface extends the internal microcontroller bus for connection of external devices.
In particular, the bus is used to connect to the external SDRAM (and optional FEEPROM).
The CTRLE functional block implements the ADSL modem command and data buffer and the interface logic supporting the various physical interfaces of the CTRLE:
- Parallel 8-bit data / 9-bit address bus (Intel or Motorola compatible)
- Serial bus (SPI-Like)

DMT Modem Description

The following essentially describes the sequence of actions for the receive direction, corresponding functions for the transmit direction are readily derived.

DSP Front-End

The DSP Front-End contains 4 parts in the receive direction: the Input Selector, the Analog Front-End Interface, the Decimator and the Time Equalizer.
The input selector is used internally to enable test loopbacks inside the chip.
The Analog Front-End Interface transfers 1 6-bits word, multiplexed on 4 input/output signals. As a result, 4 clock cycles are needed to transfer 1 word. The Decimator receives the 16-bits samples at 8.8 MHz (as sent by the Analog Front-End chip) and reduces thisrate to 2.2 MHz. The Time Equalizer (TEQ) module is an FIR filter with programmable coefficients.

Its main purpose is to reduce the effect of Inter-Symbol Interferences (ISI) by shortening the channel impulse response. Both the Decimator and TEQ can be bypassed. In the transmit direction, the DSP Front-End includes: sidelobe filtering, clipping, delay equalization and interpolation. The sidelobe filtering and delay equalization are implemented by IIR filters, reducing the effect of echo in FDM systems. Clipping is a statistical process limiting the amplitude of the output signal, optimizing the dynamic range of the AFE. The interpolator receives data at 2.2 MHz and generates samples at a rate of 8.8 MHz.

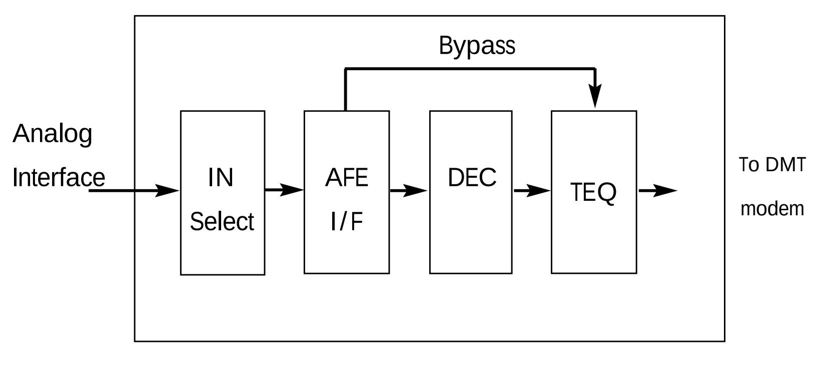

Fig.2: DSP Front-End

DMT Modem

This computational module is a programmable DSP unit. Its instruction set enables functions like FFT, IFFT, Scaling, Rotor and Frequency Equalization (FEQ). This block implements the core of the DMT algorithm as specified in ANSI T1.413. In the RX path, the 512-point FFT transforms the time-domain DMT symbol into a frequency domain representation which can be further decoded by the subsequent demapping stages. After the first stage time -domain equalization and FFT block an essentially ICI (InterCarrier Interference)-free carrier information stream has been obtained.

This stream is still affected by carrier-specific channel distortion resulting in an attenuation of the signal amplitude and a rotation of the signal phase. To compensate for these effects, the FFT is followed by a Frequency domain equalizer (FEQ) and a Rotor (phase shifter).

In the TX path, the IFFT transforms the DMT symbol generated in the frequency domain by the mapper into a time domain representation. The IFFT block is preceded by a Fine Tune Gain and a Rotor stage, allowing for a compensation of the possible frequency mismatch between the master clock frequency and the transmitter clock frequency (which may be locked to another reference).

The FFT module is a slave DSP engine controlled by the transceiver controller. It works off line and communicates with the other blocks via buffers controlled by the DSTU block. The DSP executes a program stored in a RAM area, a very flexible implementation open for future enhancements.

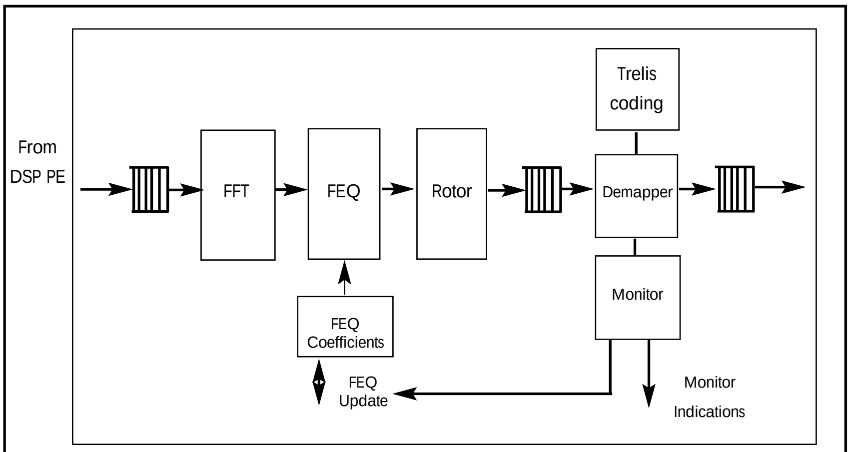

Fig.3: DMT Modem

DPLL

The Digital PLL module receives a metric for the phase error of the pilot tone. In general, the clock frequencies at the transmitter and receiver do not match exactly. The phase error is filtered and integrated by a low pass filter, yielding an estimation of the frequency offset. Various processes can use this estimate to deal with the frequency mismatch. In particular, small accumulated phase error can be compensated in the frequency domain by a rotation of the received code constellation (Rotor). Larger errors are compensated in the time domain by inserting or deleting clock cycles in the sample input sequence.

Mapper / Demapper, Monitor, Trellis Coding, FEQ Update

The Demapper converts the constellation points computed by the FFT to a block of bits. This essentially consists in identifying a point in a 2D QAM constellation plane.
The Demapper supports trellis coded demodulation and provides a Viterbi maximum likelihood estimator. When the trellis is active, the Demapper receives an indication for the most likely constellation subset to be used.
In the transmit direction, the Mapper performs the inverse operation, mapping a block of bits into one constellation point (in a complex x+jy representation) which is passed to the IFFT block. The Trellis Encoder generates redundant bits to improve the robustness of the transmission, using a 4-Dimensional Trellis Coded Modulation scheme.
The Monitor computes error parameters for carriers specified in the Demapper process. Those parameters can be used for updates of adaptive filters coefficients, clock phase adjustments, error detection,etc. A series of values is constantly monitored, such as signal power, pilot phase deviations, symbol erasures generation, loss of frame,etc.

Generic TC Layer Functions

These functions relate to byte oriented data streams. They are completely described in ANSI T1.413. Additions described in the Issue 2 of this specification are also supported.
The data received from the demapper is split into two paths, one dedicated to an interleaved data flow, the other one for a non-interleaved data flow. These data flows are also referred to as slow and fast data flows. The interleaving / deinterleaving is used to increase the error correcting capability of block codes for error bursts. After deinterleaving (if applicable), the data flow enters a Reed-Solomon error correcting code decoder, able to correct a number of bytes containing bit errors.
The decoder also uses the information of previous receiving stages that may have detected the errored bytes and have labelled them with an "erasure" indication. Each time the RS decoder detects and corrects errors in a RS codeword, an RS correction event is generated. The occurrence of such events can be signalled to the management layer. After leaving the RS decoder, the corrected byte stream is descrambled in the PMD (Physical Medium Dependent) descramblers. Two descramblers are used, for interleaved and non-interleaved data flows. These are defined in ANSI T1.413.
After descrambling, the data flows enter the Deframer that extracts and processes bytes to support Physical layer related functions according to ANSI T1.413. The ADSL frames indeed contain physical layer-related information in addition to the data passed to the higher layers. In particular, the deframer extracts the EOC (Embedded Operations Channel), the AOC (ADSL Overhead Control) and the indicators bits and passes them to the appropriate processing unit (e.g. the transceiver controller).

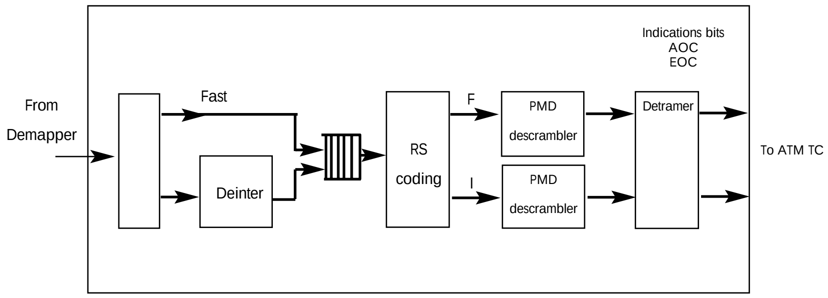

Fig.4: Generic TC Layer Functions

The deframer also performs a CRC check (Cyclic Redundancy Check) on the received frame and generates events in case of error detection. Event counters can be read by management processes. The outputs of the deframer are an interleaved and a fast data streams. These data streams can either carry ATM cells or another type of traffic. In the latter case, the ATM specific TC layer functional block, described hereafter, is bypassed and the data stream is directly presented at the input of the Interface module.

ATM Specific TC Layer Functions

The 2 bytes streams (fast and slow) are received from the byte-based processing unit. When ATM cells are transported, this block provides basic cell functions such as cell synchronization, cell payload descrambling, idle / unassigned cell filter, cell Header Error Correction (HEC) and detection. The cell processing happens according to ITU-T I.163 standard. Provision is also made for BER measurements at this ATM cell level.
When non cell oriented byte streams are transported, the cell processing unit is not active.

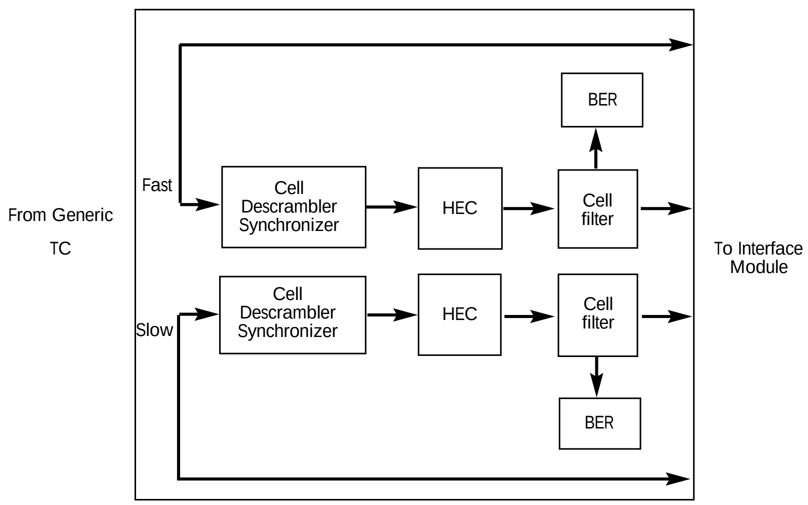

Fig.5: ATM Specific TC Layer Functions

Interface Module

The DSTU interfaces with various modules, like DSP Front-End, FFT/IFFT, Mapper/Demapper, RS , Monitor and Transceiver Controller. It consists of a real time and a scheduler modules. The real time unit generate a timebase for the DMT symbols (sample counter), superframes (symbol counter) and hyperframes (sync counter). The timebases can be modified by various control features. They are continuously fine-tuned by the DPLL module.
The DSTU schedulers execute a program, controlled by program opcodes and a set of variables, the most important of which are real time counters.The transmit and receive sequencers are completely independent and run different programs. An independent set of variables is assigned to each of them. The sequencer programs can be updated in real time.
The interface module collects cells (from the cell-based function module) or a byte stream (from the deframer). Cells are stored in FIFO's (424 bytes or 8 cells wide, transmit buffers have the same size), from which they are extracted by 2 interface submodules, one providing an Utopia level 1 interface and the other an Utopia level 2 interface.
Only one type of interface can be enabled in a specific configuration.

DMT Symbol Timing Unit (DSTU)

The DSTU interfaces with various modules, like DSP Front-End, FFT/IFFT, Mapper/Demapper, RS , Monitor and Transceiver Controller. It consists of a real time and a scheduler modules. The real time unit generate a timebase for the DMT symbols (sample counter), superframes (symbol counter) and hyperframes (sync counter). The timebases can be modified by various control features. They are continuously fine-tuned by the DPLL module.
The DSTU schedulers execute a program, controlled by program opcodes and a set of variables, the most important of which are real time counters.The transmit and receive sequencers are completely independent and run different programs. An independent set of variables is assigned to each of them. The sequencer programs can beupdated in real time.

Interfaces Analog Front-End Control Interface

The Analog Front-End Interface is designed to be connected to the MTC-20144 Analog Front-End component. Transmit Interface The 16 bit words are multiplexed on 4 AFTXD output signals. As a result 4 cycles are needed to transfer 1 word. Refer to Table 1 for the bit/pin allocation for the 4 cycles. The first of 4 cycles is identified by the CLWD signal. Refer to Figure 6. The MTC-20146 fetches the 16 bit word to be multiplexed on AFTXD from the Tx Digital Front-End module.

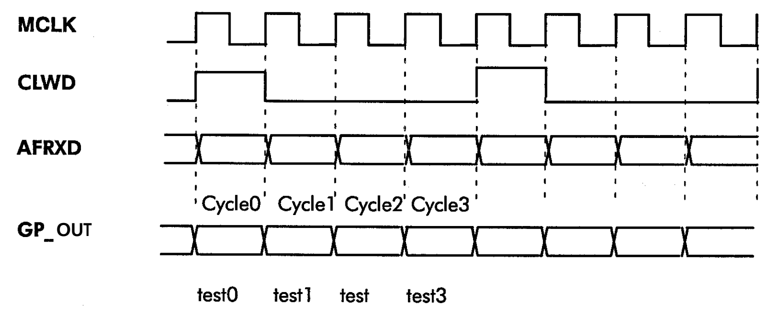

Fig.6: Timing Diagram

Table 1: Transmitted Bits Assigned to Signal/Time Slot

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFTXD [0]	b0	b4	b8	b12
AFTXD [1]	b1	b5	b9	b13
AFTXD [0]	b2	b6	b10	b14
AFTXD [0]	b3	b7	b11	b15
GP_OUT	t0	t1	t2	t3

Receive Interface

The 16 bit receive word is multiplexed on 4 AFRXD input signals. As a result 4 cycles are needed to transfer 1 word. Refer to Table 2 for the bit/pin allocation for the 4 cycles. The first of 4 cycles is identified by the CLWD signal. Refer to Figure 7. The CLWD must repeat after 4 MCLK cycles.

Master Clock (MCLK)
Analog Front End Interface Timing.

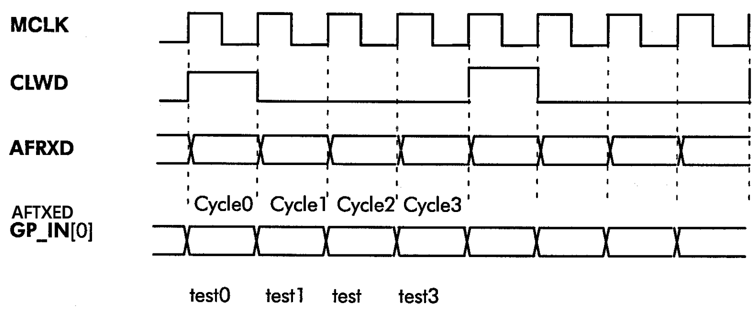

Fig.7: Receive Word Timing Diagram

Table 2: Transmitted Bits Assigned to Signal/Time Slot

	Cycle 0	Cycle 1	Cycle 2	Cycle 3
AFRXD [0]	b0	b4	b8	b12
AFRXD [1]	b1	b5	b9	b13
AFRXD [0]	b2	b6	b10	b14
AFRXD [0]	b3	b7	b11	b15

Table 3: MCLK, AC Electrical Characteristics

Symbol	Parameter	Test Cond.	Min	Typ	Max	Unit
F	Clock Frequency			35,328		MHz
Tp	Clock Period			28,3		ns
Tn	Clock data cycle			40	60	%

Transmit Interface

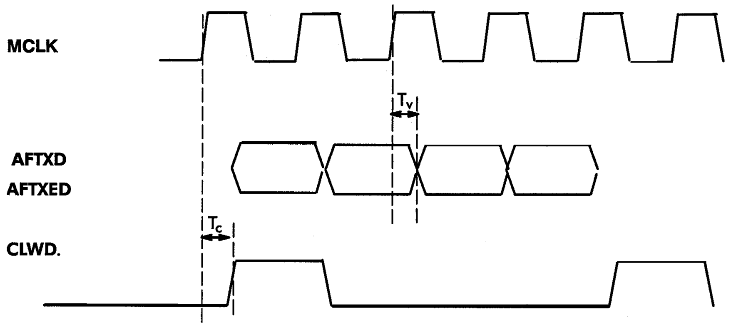

Fig. 8 : Transmit Interface

Table 4: AFTXD, AFTXED CLWD, AC Electrical Characterisitics

Symbol	Parameter	Test Cond.	Min	Typ	Max	Unit
Tv	Data valid time		0		10	ns
Tc	Data valid time		0		10	ns

Receive Interface

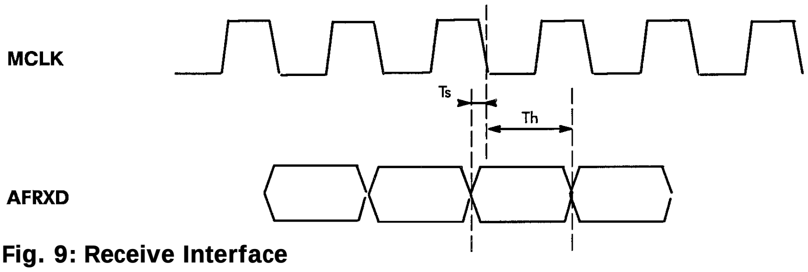

Fig. 9: Receive Interface

Table 5: AFTXD, AFTXED CLWD, AC Electrical Characterisitics

Symbol	Parameter	Test Cond.	Min	Typ	Max	Unit
Ts	Data setup time		5		10	ns
Th	Data hold time		5		10	ns

Digital Interface

Utopia Level 2 Interface
The ATM forum takes the ATM layer chip as a reference. It defines the direction from ATM to physical layer as the Transmit direction. The direction from physical layer to ATM as the Receive direction is referred to as the receive direction. Figure 10 shows the interconnection between ATM and PHY layer devices, the optional signals are not supported and not shown.
The UTOPIA interface transfers one byte in a single clock cycle, as a result cells are transferred in 53 clock cycles. Both transmit and receive interfaces are synchronized on clocks generated by the ATM layer chip, and no specific relationship between Receive and Transmit clock is assumed, they must be regarded as mutually asynchronous clocks. Flow control signals are available to match the bandwidth constraints of the physical layer and the ATM layer.
The UTOPIA level 2 supports point to multi point configurations by introducing an addressing capability and by making a distinction between polling and selecting a device :
- the ATM chip polls a specific physical layer chip by putting its address on the address bus when the Enb line is asserted. The addressed physical layer answers the next cycle via a Clav line reflecting its status at that time.
- the ATM chip selects a specific physical layer chip by putting its address on the address bus when the Enb line is deasserted and asserting the Enb line on the next cycle. The addressed physical layer chip will be the target or source of the next cell transfer.
Reference Spec: Utopia Specification Level 2, Version 1.0, June 95.
See www.atmforum.com

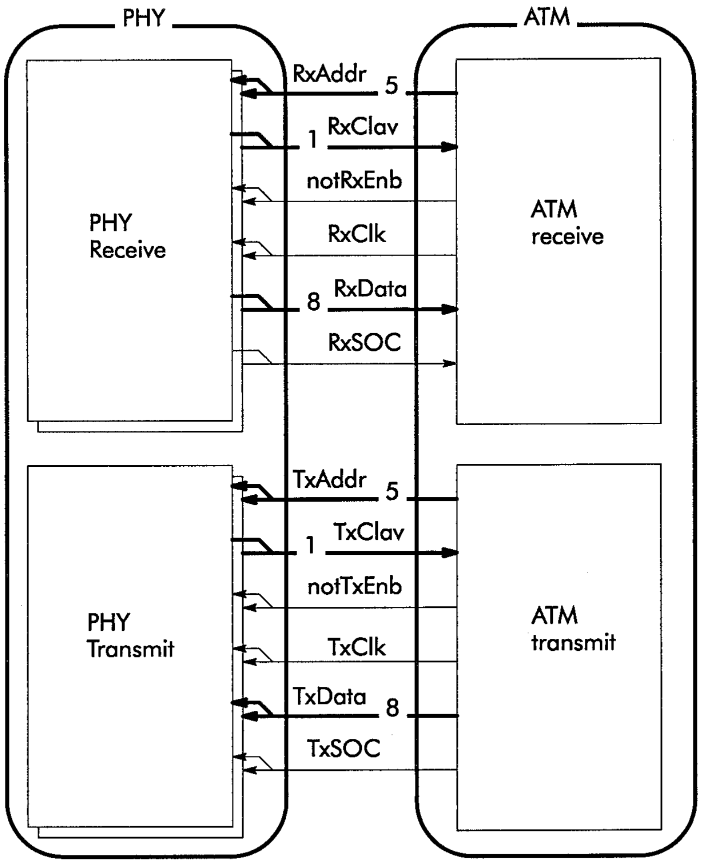

Fig. 10: Signals at Utopia Level 2 interface

Table 6: Signal Definitions for the Utopia Receive Path

Name	Meaning	Usage	Remark
RxClav	Receive Cell available	Signals that the ATM chip that the physical layer chip has a call ready for transfer.	Remains active for the entire cell transfer.
notRxEnb	Receive Enable (Active low)	Signals to the physical layer chip that the ATM layer chip will sample and accept data during next clock cycle.	RxData and RxSOC could be tristate when notRxEnb is inactive (high).
RxCx	Receive Byte Clock	Give the timing signal for the transfer, generated by ATM layer chip.	
RxData	Receive Data	ATM cell data from physical layer chip to ATM chip, byte wide.	
RxSOC	Receive Start Of Cell	Identifies the cell boudary on RxData	
RxAddr	Receive Adress	Use to select the port that will be active or polled	

UTOPIA Level 2 Signals

The physical layer chip sends cell data towards the ATM layer chip. The ATM layer chip polls the status of the FIFO of the physical layer chip. Refer to Table 6 for a list of interface signals.
The cell exchange proceeds like :
a) The physical layer chip signals the availability of a cell by asserting RxClav when polled by the ATM chip.

b) The ATM chips selects a physical layer chip, then starts the transfer by asserting notRxEnb.

c) If the physical layer chip has data to send, it puts them on the RxData line the cycle after it sampled notRxEnb active. It also advances the offset in the cell. If the data transferred is the first byte of a cell, RxSOC is 1b at the time of the data transfer, 0b otherwise.

d) The ATM chip accepts the data when they are available. If RxSOC was 1b during the transfer, it resets its internal offset pointer to the value 1, otherwise it advances the offset in the cell.

MTC-20146 Utopia Level 2 MPHY Operation

Utopia level 2 MPHY operation can be done by various interface schemes. The MTC-20146 supports only the required mode, this mode is referred to as «operation with 1 TxClav and 1 RxClav.»

PHY Device Identification

The MTC-20146 holds 2 PHY layer Utopia ports, one is dedicated to the fast data channel, the other one to the interleaved data channel. The associated PHY address is specified by the PHY_ADDR_x fields the Utopia PHY address register. Beware that an incorrect address configuration may lead to bus conflicts. A feature is defined to disable (tri-state) all outputs of the Utopia interface. It is enabled by the TRI_STATE_EN bit in the Rx_Interface control register.
Utopia Level 1 Data Flow Selection
In this mode the MTC-20146 can only support one data flow (either fast or interleaved). The selection between fast or interleaved is under control of the Transceiver Controller.
Utopia Level 1 Configuration
MTC-20146
Reference Spec: Utopia Specification Level 1, Version 2.0, March 94.
See www.atmforum.com

Table 7: Signal Definitions for the Utopia Transmit Path

Name	Meaning	Usage
TxClav	Transmit Cell available	Signals to the ATM chip that the physical layer chip is ready to accept a call.
notTxEnb	Transmit Enable (Active low)	Signals to the physical layer chip that TxData and TxSOC are valid.
TxCx	Transmit Byte Clock	Gaves the timing signal for the transfer, generated by ATM layer chip.
TxData	Transmit Data	ATM cell data from ATM chip to physical layer chip, byte wide.
TxSOC	Transmit Start Of Cell	Identifies the cell boudary on TxData
TxAddr	Transmit Adress	Use to select the port that will be

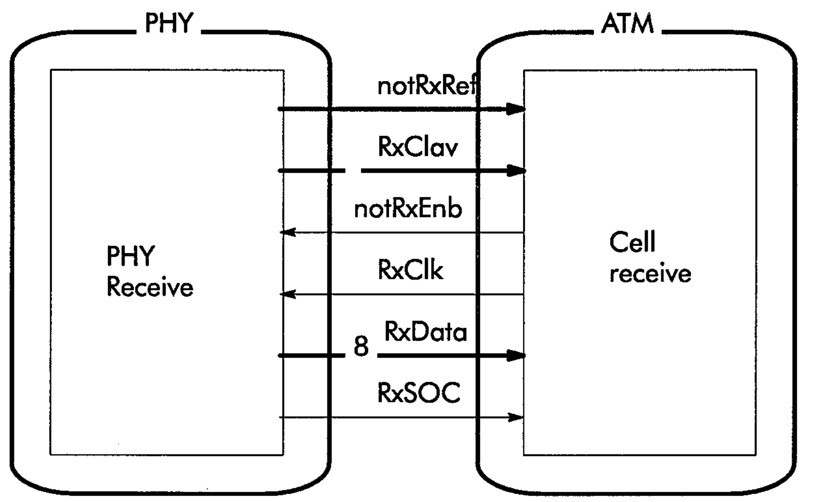

Fig. 11: Signals at Utopia Level 1 interface

Utopia Level 1 Handshake Protocol PHY->ATM.

The MTC-20146 supports a cell level handshake protocol only. The ATM layer indicates it wants to read data by asserting the notRxEnb signal. The PHY layer dumps 53 bytes (1 cell) on the RxDATA bus, a cell start indication is available on the RxSOC signal. Refer to Figures 12.

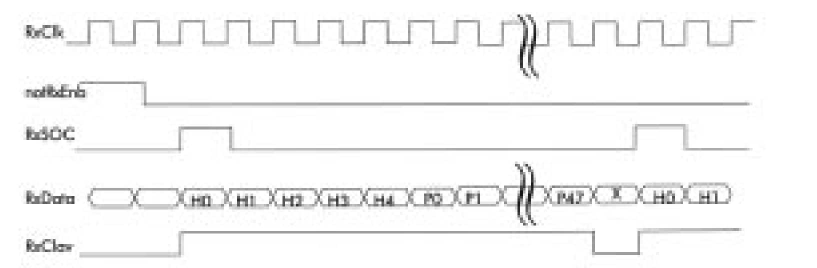

Fig.12a: Utopia Level 1 Functional Timing Diagram (PHY -> ATM)

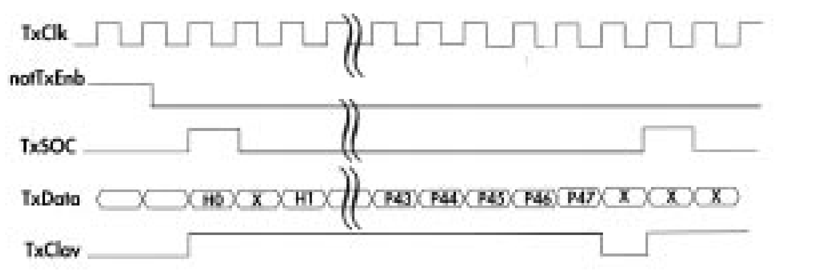

Fig.12b: Utopia Level 1 Functional Timing Diagram (ATM -> PHY)

Table 8: Utopia level 1 Pinout

Name signal	Type	Pin
RxData	0	U_RxData
RxSOC	0	U_RxSOC
notRxEnb	1	U_RxENBB
RxClav	0	U_RxCLAV
RxClk	1	U_RxCLK

Table 9: U_TxCLK, U_RxCLK, AC Electrical Characteristics

Symbol	Parameter	Test Cond.	Min	Typ	Max	Unit
F	Clock Frequency		1.5		25	MHz
Tc	Clock duty cycle		40		60	%
Tj	Clock peak to peak jitter				5	%
Trf	Clock rise / fall time				4	ns
L	Load				100	pF

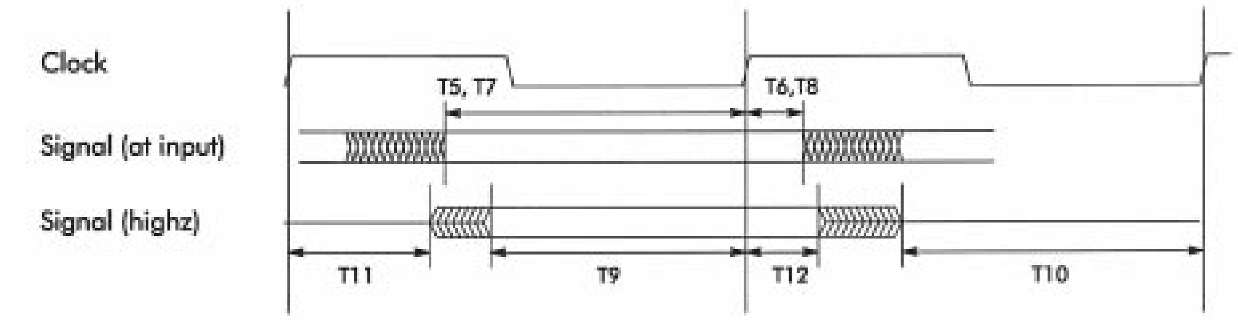

Fig.13: Utopia Timing Diagram

Table 10: U_RxADDR AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T5	Input setup time to U_RxCLK	10			ns
Tß	Hold time time to U_RxCLK	1			ns
L	load			100	pf

Table 11: U_RxData, U_RxSOC, U_RxClav AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T7	Input setup time to U_TxCLK	10			ns
T8	Hold time time to U_TxCLK	1			ns
T9	Signal going low impedance to U_RxCLK	10			ns
T10	Signal going high impedance to U_RxCLK	0			ns
T11	Signal going low impedance to U_RxCLK	1			ns
T12	Signal going high impedance to U_RxCLK	1			ns
L	Load			100	pf

Table 12: U_RxADDR AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T7	Input setup time to U_TxCLK	10			ns
T8	Hold time time to U_TxCLK	1			ns
T9	Signal going low impedance to U_RxCLK	10			ns
T10	Signal going high impedance to U_RxCLK	0			ns
T11	Signal going low impedance to U_RxCLK	1			ns
T12	Signal going high impedance to U_RxCLK	1			ns
L	Load			100	pf

Peripherals

The peripherals block includes two UARTS for RS232 interfacing to external systems and two general purpose parallel I/O lines.

Miscellaneous

This includes the clock circuitry, reset circuitry, test functions and configuration control signals.

SDRAM

The SDRAM interface allows a glueless interconnection of 1 SDRAM 1Mx16, of type uPD4516161 or compatible. Following features are provided for SDRAM access.

-16 bit databus and 12 bit address bus.

-Control signals : S_nCS, S_nRAS, S_nCAS, S_nWE, S_DQM[1:0}

Control signal timing

All SDRAM actions are triggered at the rising edge of its clock.

Timing diagrams for a burst of four 16-bit accesses to 16-bit SDRAM (Figure 14 and Figure 15) show the basic behavior of the control signals.

Memory

Following features are provided for memory access (SRAM or FEPROM) :

- 16 bit databus and 20 bit address bus giving 1Mbyte address space per chip select
- Control signals : E_nCS[0:1], E_nOE, E_nWE0, E_nWE1
- Setup and wait state insertion
- 8, 16 and 32 bit access by MTC-20146 to 8 or 16 bit memory according to little endian convention

EBI Interface Timing

All timing parameters are specified at a load of 100 pF, all the electrical levels are CMOS compatible.

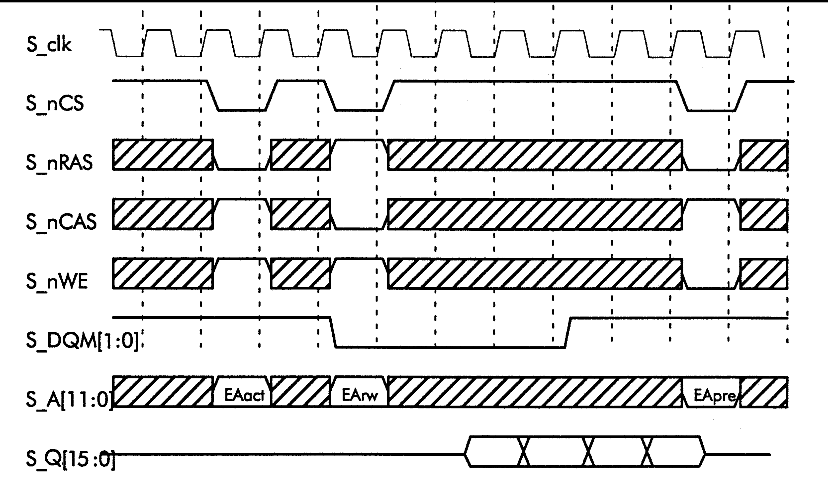

Fig. 14: SDRAM read access (CAS latency=3; Burst length=4)

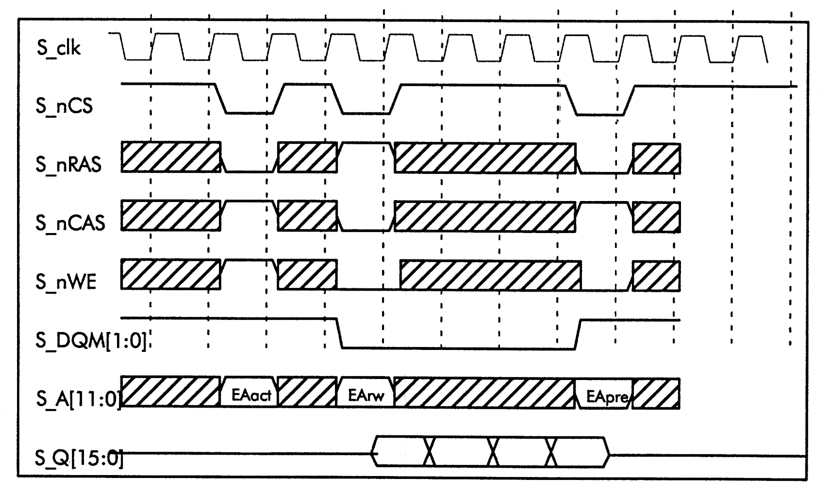

Fig. 15: SDRAM write access (CAS latency=3; Burst length=4)

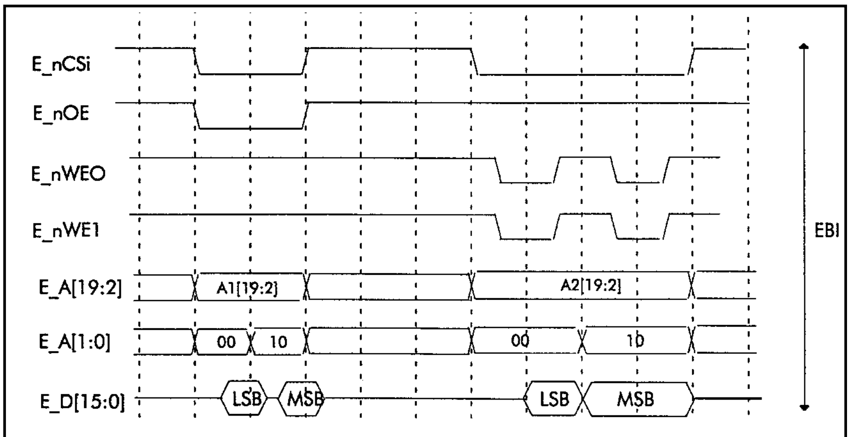

Fig. 16: EBI memory access (32-bit Word R/W to 16 bit memory), maximum speed timing

CTRLE

The Ctrl-E interface is an ADSL-oriented mailbox system to exchange control and status messages between MTC-20146 and an external controller. It consists of a mailbox and a physical interface.
The mailbox has two 8-bit command registers to pass commands from the MTC-20146 internal controller bus (ASB) to Ctrl-E (RxCommand) and from Ctrl-E to
ASB (TxCommand), and two status registers (RxComAv and TxComAv) to indicate the status of the command register. Data associated with a command can be exchanged using a common CtrleDataBuffer. A hardware semaphore mechanism is provided to allow control of data consistency of the CtrleDataBuffer.
The Ctrl-E physical interface between the mailbox and an external controller can be used in one of two modes : as a dedicated serial bus interface or as a generic parallel bus interface. Selection between serial and parallel mode is done with an external mode strap, IO pins are shared.

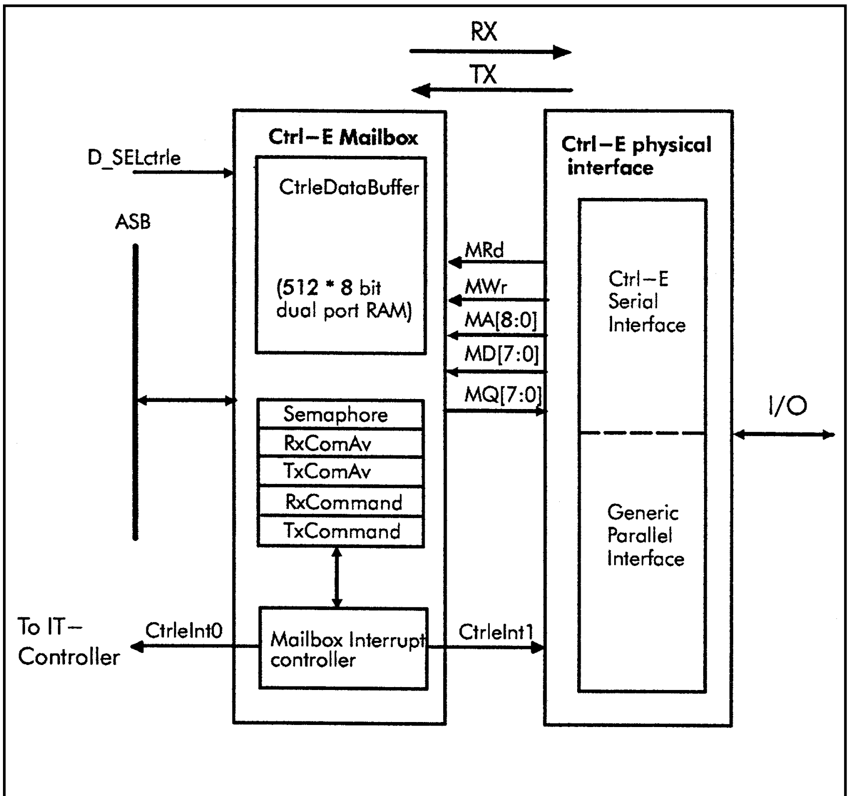

Fig.17: Ctrl-E Interface Controller principle

Ctrl-E Mailbox
The Ctrl-E Mailbox occupies a 512 byte memory map accessible by the Ctrl-E physical interface and by the ASB bus. The mailbox memory map is given in Table 13.
An external interrupt can be generated by the Mailbox interrupt controller.
À full description of the CTRLE protocol and use of the CTRLE mailbox is available in the "Modem control Interface Specifications" documents, available separately.

Ctrl-E Semaphore
A simple semaphore mechanism is provided to allow control of the data consistency of the CtrleDataBuffer. One mailbox address is defined as a two-bit semaphore register protected by control logic to prevent unallowed write accesses to this register.
Before the databuffer is read or written by one of the two interfaces (ASB or Ctrl-E) this interface should perform a 'P-operation' on the semaphore. After a

Table 13: Ctrl-E controller memory map:

Field	ACC	Mailbox Address MA[8:0]	Size (bit)	Initial	Function
TxCommand	Rw	000h	8	00h	Command written by Ctrl-E, read by ASB
RxCommand	Rw	001h	8	00h	Command written by ASB, read by Ctrl-E
TxComAv	Rw	002h	1	0lb	1-bit register: 1 if TX command available
RxComAv	Rw	003h	1	0lb	1-bit register: 1 if RX command available
Semaphore	PV	004h	2	00b	Semaphore for access read by Ctrl-E
CtrleDataBuffer	Rw	005h-1FFh	8	00h	507x8 bit data buffer

Table 14: Semaphore Pand V operations:
new value after write by ASB or Ctrl-E

Semaphore operation	originator	write value	previous semaphore value		
			semaphore free	semaphore taken by ASB	Ctrl-E
			00b	01b	11b
P	ASB	01b	01b	01b	11b
	Ctrl-E	11b	11b	01b	11b
V	ASB	00b	00b	00b	11b

read or write of the databuffer the interface should do a ’V-operation’ releasing the semaphore. P and V operations are performed by write and read accesses to the semaphore register. The semaphore will be updated as shown in Table 14.
Each semaphore operation (P or V) consists of two consecutive actions that don’t have to be atomic :
a) Write the correct value to the semaphore address (see Table 14)
b) Read the value in the semaphore address.
If the value read is different from the value writen the P or V operation was not succesfull and should be tried again.

The databuffers can be accessed without using the semaphore mechanism if data consistency is guaranteed in another way. If other values are written to the semaphore address than the values listed the write will not be performed.

Ctrl-E Physical Interface

A generic parallel interface with 9 bit Address and 8 bit Data bus is implemented two parallel bus modes are defined to support both Motorola-compatible and Intel-compatible timing and control signals. This interface specifi-cation is compliant to Utopia Level 2 Parallel Management Interface. bus mode is done with the C_Mode input pin :

Generic Parallel Interface
The two parallel bus modes differ only in the definition of 3 control signals : busmode 0 provides a read / write selector, a data strobe and a ready acknowledge. Busmode 1 provides a read strobe, a write strobe and a ready acknowledge. The signal definition is shown in following table :

Table 15: Ctrl-E interface signals in parallel interface modes

Signal name	Type	Function	PIN
C_A[8:0]	I	address bus	C_A[8:0]
C_D[7:0]	I0	byte wide bidirectional data bus	C_D[7:0]
C_notCS	I	chip select	C_notCS
C_notnt	0Z	Interrupt output, derived from CtrleInt1 signal from Mailbox: low when CtrleInt1 is low, else tristated	C_notnt
Mode 0: Motorola-compatible mode			
C_Mode[1:0]	I	0Db	C_Mode[1:0]
C_Rd / notWr	I	read acces if 1, write acces if 0	C_notWr
C_not DS	I	Data Strobe	C_notRd
C_not DtAcx	OZ	Bus cycle ready indication, indicates that data on bus can be sampled or removed	C_notRdy
Mode 1: Intel-compatible mode			
C_Mode[1:0]	I	01b	C_Mode[1:0]
C_notWr	I	write cycle indication	C_notWr
C_notRd	I	read cycle indication	C_notRd
C_notRdy	OZ	Bus cycle ready indication, indicates that data on bus can be sampled or removed, same as in mode 0	C_notRdy

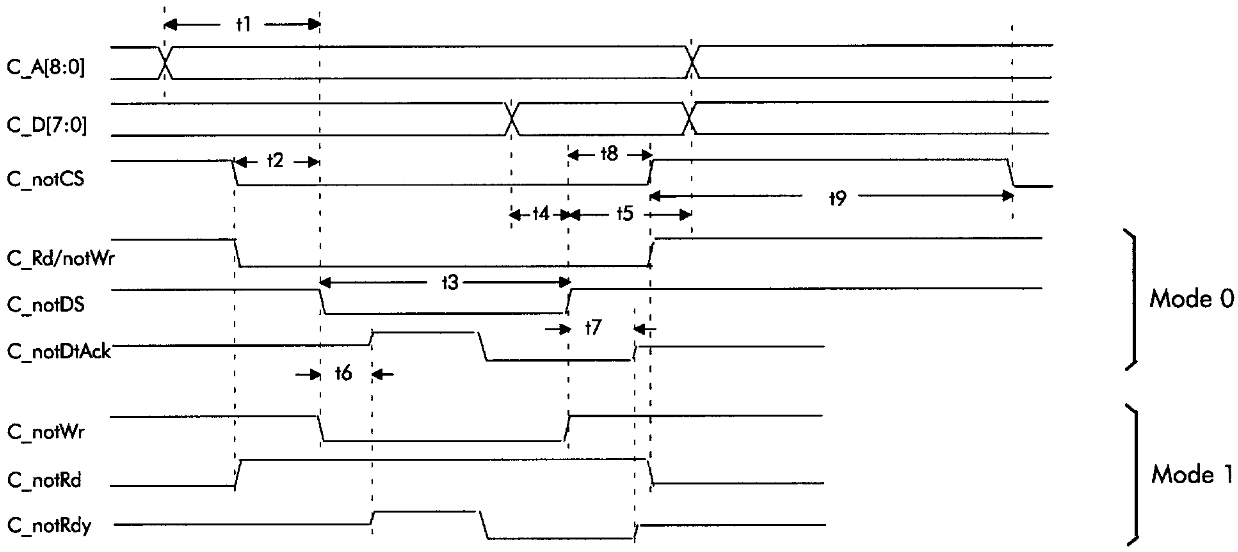

Fig. 18: Ctrl-E Interface write cycle timing in parallel modes 0 and 1

Table 16: Ctrl-E interface signals in parallel interface modes

Symbol	Description	Min	Max	Unit
t1	C_A Setup to C_notDS (C_notWr) low	0		ns
t2	C_notCS, C_Rd/notWr setup to C_notDS (C_notWr) low	0		ns
t3	C_notDS (C_notWr) pulse width	215		ns
t4	C_D setup to C_notDS (C_notWr) high	15		ns
t5	C_A, C_D hold from C_notDS (C_notWr) high	5		ns
t6	C_notDtAck (C_notRdy) valid from C_notDS (C_notWr) low		15	ns
t7	C_notDtAck (C_notRdy) tri-state from C_notDS (C_notWr) high		15	ns
t8	C_notCS, C_Rd/notWr hold from C_notDS (C_notWr) high	0		ns
t9	C_notCS high to C_notCS Low	100		ns

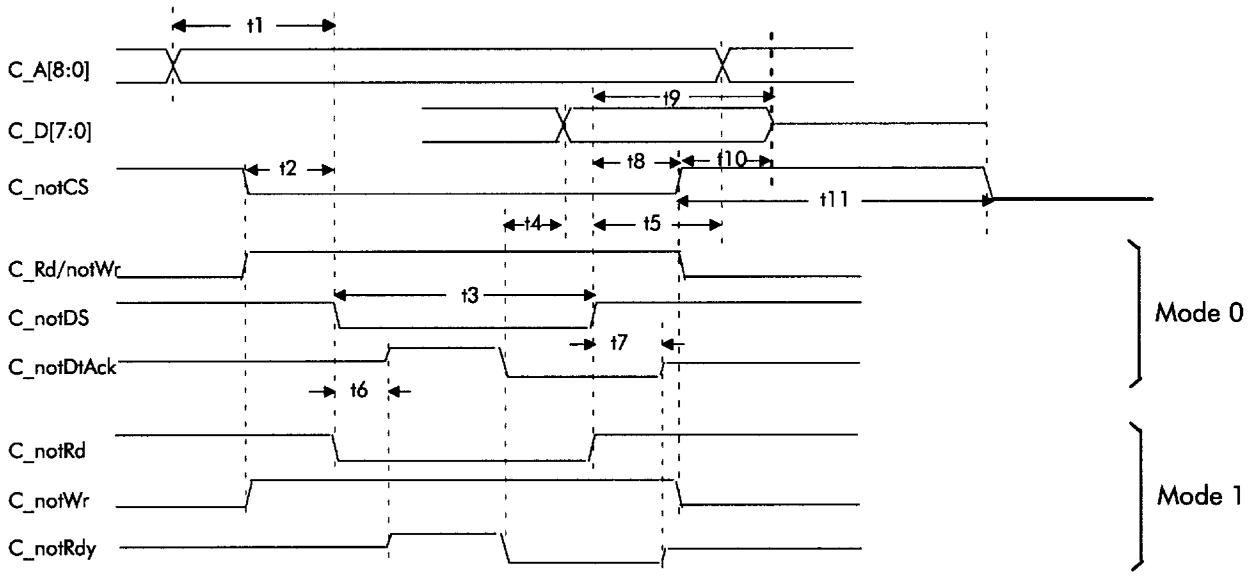

Fig. 19: Ctrl-E Interface read cycle timing in parallel modes 0 and 1

Table 17: Read cycle timing in parallel modes 0 and 1

Symbol	Description	Min	Max	Unit
t1	C_A Setup to C_notDS (C_notRd) low	0		ns
t2	C_notCS, C_Rd/notWr setup to C_notDS (C_notRd) low	0		ns
t3	C_notDS (C_notRd) pulse width	215		ns
t4	C_D valid from C_notDtAck (C_notRdy) low		10	ns
t5	C_A, hold from C_notDS (C_notRd) high	0		ns
t6	C_notDtAck (C_notRdy) valid from C_notDS (C_notRd) high		15	ns
t7	C_notDtAck (C_notRdy) tri-state from C_notDS (C_notRd) high		10	ns
t8	C_notCS, C_Rd/notWr hold from C_notDS (C_notRd) high	10		ns
t9	Data tri-state from C_notDS (C_notRd) high	90	100	ns
t10	Data tri-state from C_notCS high	5	15	ns
t11	C_notCS high to C_notCS low (Min. time between 2 Accesses)	100		ns

Electrical Specifications
Generic

The values presented in the following table apply for all inputs and / or outputs unless specified otherwise. Specifically they are not influenced by the choice between CMOS or TTL levels.

Table 18: IO buffers generic DC characteristics MTC-20146

DC Electrical Characteristics All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**type**	**Max**	**Unit**
LN	Input leakage current	VIN = VSS.VDD.no pull up / pull down	1		1	µA
LOZ	Tristate leakage current	VIN = VSS.VDD.no pull up / pull down	1		1	µA
IPU	Pull up current	VIN = VSS	25	66	125	µA
IPD	Pull down current	VIN = VDD	25	66	125	µA
APU	Pull up resistance	VIN = VSS		50		kOhm
APU	Pull down resistance	VIN = VDD		50		kOhm

Table 19: IO buffers dynamic characteristics MTC-20146

DC Electrical Characteristics All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**type**	**Max**	**Unit**
CIN	Input capacitance	@f=1MHz			5	pF
dI / dt	Current derivative	8 mA driver, slow rate control 8 mA driver, no slow rate control		23,5 89		mA / ns mA / ns
Ipeak	Peak current	8 mA driver, slow rate control 8 mA driver, no slow rate control		85 100		mA mA
COUT	Output capacitance (also bidirectional and tristate driver)	@f=1MHz			7	pf

Input / Output CMOS Generic Characteristics

The values presented in the following table apply for all CMOS inputs and / or outputs unless specified otherwise.

Table 20: CMOS IO buffers generic characterisitics MTC-20146

DC Electrical Characteristics
All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage				0,2'' V_{DD}	V
VIH	High level input voltage		0,8*V_{DD}			V
VHY	Schmitt triger hysteresis	slow edge < 1 V / ms, only for SCHMITx	0.8			V
VOL	Low level output voltage	L_{OUT} = Xmal			0.4	V
VOH	High level output voltage	L_{OUT} = Xmal	0.85*VDD			V

Input / Output TTL Generic Characteristics

The values presented in the following table apply for all TTL inputs and / or outputs unless specified otherwise.

Table 21: TTL IO buffers generic characterisitics MTC-20146

DC Electrical Characteristics
All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage				0.8	V
VIH	High level input voltage		2.0			V
VILHY	Low level threshold, falling	slow edge < 1 V / ms	0.9		1.35	V
VIHHY	High level threshold, rising	slow edge < 1 V / ms	1.3		1.9	V
VHY	Schmitt trigger hysteresis	slow edge < 1 V / ms	0.4		0.7	V
VOL	Low level output voltage	L_{OUT} = Xma1			0.4	V
VOH	High level output voltage	L_{OUT} = -Xma1	2.4			V

Operating Conditions

Table 22: Operating Conditions

DC Electrical Characteristics All voltages are referenced to VSS, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
VDD -IO	Supply voltage IO		3.0	3.3	3.6	V
TA	Ambient temperature Tm/s airflow		.40		+85	C
P	Power dissipation			300	400	mW
VDD-CORE			3	3.3	3.6	V

Package and Pinning

TQFP176

NO.	Pin Name	Dir funct	Dir test	pad type	Description
1	TDI	in	in	IBUFUQ	test data in
2	CARM_RESETN	in		SCHMITC	carm reset signal, active low
3	nCS_0	out		B8CR	CS signal for flash eprom
4	VSS_IO			VSSI	IO ground
5	VDD_IO			VDDI	IO +3.3V power supply
6	T_ACK	out		B4CR	test acknowledge
7	T_REQB	in		IBUFDQ	test request signal
8	T_REQA	in		IBUFDQ	test request signal
9	TROM	in		SCHMITC	boot from test Rom select
10	PA[1]	inout	inout	BD4CR	port A bit[1]
11	PA[0]	inout	inout	BD4CR	port A bit[0]
12	VSS_CORE			VSSI	CORE ground
13	VDD_CORE			VDDI	CORE +3.3V power supply
14	PA14	inout		BD4CR	download mode select (CTRL-E or UART1)
15	PA15	inout		BD4CR	download mode select (UART baudrate)
16	E_CLK	inout	inout	BD8CR	EBI clock
17	S_nWE	out		B8CR	control signal SDRAM
18	S_nRAS	out		B8CR	control signal SDRAM
19	VSS_IO			VSSI	IO ground
20	VDD_IO			VDDI	IO +3.3V power supply
21	S_nCAS	out		B8CR	control signal SDRAM
22	S_nLDQM	out		B8CR	control signal SDRAM
23	S_nUDQM	out		B8CR	control signal SDRAM
24	E_A[15]	inout		BD8CR	adress bus / testbus MSB
25	E_A[14]	inout		BD8CR	adress bus / testbus MSB
26	VSS_IO			VSSI	IO ground
27	VDD_IO			VDDI	IO +3.3V power supply
28	E_A[13]	inout		BD8CR	adress bus / testbus MSB
29	E_A[12]	inout		BD8CR	adress bus / testbus MSB
30	E_A[11]	inout		BD8CR	adress bus / testbus MSB
31	E_A[10]	inout		BD8CR	adress bus / testbus MSB
32	E_A[9]	inout		BD8CR	adress bus / testbus MSB
33	VSS_CORE			VSSI	IO ground
34	VDD_CORE			VDDI	IO +3.3V power supply
35	E_A[8]	inout		BD8CR	adress bus / testbus MSB
36	E_A[7]	inout		BD8CR	adress bus / testbus MSB
37	E_A[6]	inout		BD8CR	adress bus / testbus MSB
38	E_A[5]	inout		BD8CR	adress bus / testbus MSB
39	E_A[4]	inout		BD8CR	adress bus / testbus MSB
40	VSS_IO			VSSI	IO ground
41	VDD_IO			VDDI	IO +3.3V power supply
42	E_A[3]	inout		BD8CR	adress bus / testbus MSB
43	E_A[2]	inout		BD8CR	adress bus / testbus MSB
44	E_A[1]	inout		BD8CR	adress bus / testbus MSB
45	E_A[0]	inout		BD8CR	adress bus / testbus MSB
46	E_D[0]	inout		BD8SCRDQ	data bus / testbus LSB
47	E_D[1]	inout		BD8SCRDQ	data bus / testbus LSB
48	VSS_IO			VSSI	IO ground
49	VDD_IO			VDDI	IO +3.3V power supply
50	E_D[2]	inout		BD8SCRDQ	data bus / testbus LSB
51	E_D[3]	inout		BD8SCRDQ	data bus / testbus LSB
52	E_D[4]	inout		BD8SCRDQ	data bus / testbus LSB
53	E_D[5]	inout		BD8SCRDQ	data bus / testbus LSB

NO.	Pin Name	Dir funct	Dir test	pad type	Description
54	E_D[6]	inout		BD8SCRDQ	data bus / testbus LSB
55	VSS_CORE			VSSI	CORE ground
56	VDD_CORE			VDDI	CORE +3.3V power supply
57	E_D[7]	inout		BD8SCRDQ	data bus / testbus LSB
58	E_D[8]	inout		BD8SCRDQ	data bus / testbus LSB
59	E_D[9]	inout		BD8SCRDQ	data bus / testbus LSB
60	E_D[10]	inout		BD8SCRDQ	data bus / testbus LSB
61	E_D[11]	inout		BD8SCRDQ	data bus / testbus LSB
62	VSS_IO			VSSI	IO ground
63	VDD_IO			VDDI	IO +3.3V power supply
64	E_D[12]	inout		BD8SCRDQ	data bus / testbus LSB
65	E_D[13]	inout		BD8SCRDQ	data bus / testbus LSB
66	E_D[14]	inout		BD8SCRDQ	data bus / testbus LSB
67	E_D[15]	inout		BD8SCRDQ	data bus / testbus LSB
68	S_nOE	out		B8CR	output enable
69	S_CS	out		B8CR	chip select signal (SDRAM)
70	VSS_IO			VSSI	IO ground
71	VDD_IO			VDDI	IO +3.3V power supply
72	AFTXD[3]	out		B8	transmit data nibble
73	AFTXD[2]	out		B8	transmit data nibble
74	AFTXD[1]	out		B8	transmit data nibble
75	AFTXD[0]	out		B8	transmit data nibble
76	IDDq	in		IBUF	test pin, active high
77	VSS_CORE			VSSI	CORE ground
78	VDD_CORE			VDDI	CORE +3.3V power supply
79	CTRLDATA	inout		BD4CR	serial data transmit channel
80	MCLK	in		SCHMITC	master clock
81	CLWD	in		IBUF	start of word indication
82	AFRXD[3]	in		IBUF	receive data nibble
83	AFRXD[2]	in		IBUF	receive data nibble
84	VSS_IO			VSSI	IO ground
85	VDD_IO			VDDI	IO +3.3V power supply
86	AFRXD[1]	in		IBUF	receive data nibble
87	AFRXD[0]	in		IBUF	receive data nibble
88	POWER_LOWB	inout		BD4CR	Power down analog front end
89	U_TxADDR[0]	in		IBUFDQ	utopia tx adress bit
90	U_TxData[0]	in		IBUF	utopia tx data bus
91	U_TxData[1]	in		IBUF	utopia tx data bus
92	VSS_IO			VSSI	IO ground
93	VDD_IO			VDDI	IO +3.3V power supply
94	U_TxData[2]	in		IBUF	utopia tx data bus
95	U_TxData[3]	in		IBUF	utopia tx data bus
96	U_TxData[4]	in		IBUF	utopia tx data bus
97	U_TxData[5]	in		IBUF	utopia tx data bus
98	U_TxData[6]	in		IBUF	utopia tx data bus
99	VSS_CORE			VSSI	CORE ground
100	VDD_CORE			VDDI	CORE +3.3V power supply
101	U_TxData[7]	in		IBUF	utopia tx data bus
102	U_TxENBB	in		IBUF	Utopia Tx enable
103	U_TxCLAV	inout		BD8SCR	Utopia Tx cell available
104	U_TxSOC	in		IBUF	transmit interface start of cell indication
105	U_TxCLK	in		IBUF	transmit interface utopia clock
106	VSS_IO			VSSI	IO ground
107	VDD_IO			VDDI	IO +3.3V power supply
108	U_RxENBB	in		IBUF	Utopia Rx enable
109	U_RxCLAV	inout		BD8SCR	Utopia Rx cell available
110	U_RxSOC	inout		BD8SCR	receive interface start of cell indication

NO.	Pin Name	Dir funct	Dir test	pad type	Description
111	U_RxCLK	in		IBUF	receive interface utopia clock
112	U_TxRefB	in		IBUFDQ	8 kHz clock from network
113	U_RxRefB	inout		BD4CR	8 kHz clock to ATM device
114	VSS_IO			VSSI	IO ground
115	VDD_IO			VDDI	IO +3.3V power supply
116	U_RxADDR[0]	in		IBUFDQ	Utopia rx adress bit
117	U_RxData[7]	outZ		BD8SCR	Utopia rx data bus
118	U_RxData[6]	outZ		BD8SCR	Utopia rx data bus
119	U_RxData[5]	outZ		BD8SCR	Utopia rx data bus
120	U_RxData[4]	outZ		BD8SCR	Utopia rx data bus
121	VSS_CORE			VSSI	CORE ground
122	VDD_CORE			VDDI	CORE +3.3V power supply
123	U_RxData[3]	outZ		BD8SCR	Utopia rx data bus
124	U_RxData[2]	outZ		BD8SCR	Utopia rx data bus
125	U_RxData[1]	outZ		BD8SCR	Utopia rx data bus
126	U_RxData[0]	outZ		BD8SCR	Utopia rx data bus
127	SACHEM_RESETB	in		IBUF	sachem hard reset, active low
128	VSS_IO			VSSI	IO ground
129	VDD_IO			VDDI	IO +3.3V power supply
130	C_A[8]	inout	inout	BD8CR	Ctrl_E adress bus
131	C_A[7]	inout	inout	BD8CR	Ctrl_E adress bus
132	C_A[6]	inout	inout	BD8CR	Ctrl_E adress bus
133	C_A[5]	inout	inout	BD8CR	Ctrl_E adress bus
134	C_A[4]	inout	inout	BD8CR	Ctrl_E adress bus
135	C_A[3]	inout	inout	BD8CR	Ctrl_E adress bus
136	VSS_IO			VSSI	IO ground
137	VDD_IO			VDDI	IO +3.3V power supply
138	C_A[2]	inout	inout	BD8CR	Ctrl_E adress bus
139	C_A[1]	inout		BD8CR	Ctrl_E adress bus
140	C_A[0]	inout		BD8CR	Ctrl_E adress bus
141	C_D[7]	inout	inout	BD8CR	Ctrl_E data bus
142	C_D[6]	inout	inout	BD8CR	Ctrl_E data bus
143	VSS_CORE			VSSI	CORE ground
144	VDD_CORE			VDDI	CORE +3.3V power supply
145	C_D[5]	inout	inout	BD8CR	Ctrl_E data bus
146	C_D[4]	inout	inout	BD8CR	Ctrl_E data bus
147	C_D[3]	inout	inout	BD8CR	Ctrl_E data bus
148	C_D[2]	inout		BD8CR	Ctrl_E data bus
149	C_D[1]	inout		BD8CR	Ctrl_E data bus
150	VSS_IO			VSSI	IO ground
151	VDD_IO			VDDI	IO +3.3V power supply
152	C_D[0]	inout		BD8CR	Ctrl_E data bus
153	C_clk	in		SCHMITC	Ctrl_E serial input clock
154	C_notCS	in		SCHMITC	Ctrl_E chip select
155	C_notWr	in		SCHMITC	Ctrl_E write indication
156	C_notRd	inout		BD4CR	Ctrl_E read indication
157	VSS_IO			VSSI	IO ground
158	VDD_IO			VDDI	IO +3.3V power supply
159	C_notRdy	out_Hiz		BT4CR	Ctrl_E ready indication
160	C_notInt	out_Hiz		BT4CR	Ctrl_E interface interrupt
161	MODE[1]	in		IBUF	select functionnal and test mode
162	MODE[0]	in		IBUF	select functionnal and test mode
163	SCAN_CLK	in		SCHMITC	scan clock
164	VSS_CORE			VSSI	CORE ground
165	VDD_CORE			VDDI	CORE +3.3V power supply
166	TESTSE	in	in	SCHMITCDQ	test scan enable
167	RSRXD1	inout		BD4CR	serial Rx port

NO.	Pin Name	Dir funct	Dir test	pad type	Description
168	RSTXD1	inout		BD4CR	serial Tx port
169	C_mode[0]	in		SCHMITCDQ	Ctrl-E mode signal : 0=motorola, 1=intel
170	GP	inout		BD4CR	carm iddq pin
171	TCK	in	in	IBUFUQ	jtag clock
172	VSS_IO			VSSI	IO ground
173	VDD_IO			VDDI	IO +3.3V power supply
174	nTRST	in	in	IBUFDQ	reset jtag interface
175	TMS	in	in	IBUFUQ	test mode select
176	TDO	out	out	BT4CR	test data o

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NO.	Pin Name	Dir funct	Dir test	pad type	Description
1	TDI	in	in	IBUFUQ	test data in
2	CARM_RESETN	in		SCHMITC	carm reset signal, active low
3	nCS_0	out		B8CR	CS signal for flash eprom
4	VSS_IO			VSSI	IO ground
5	VDD_IO			VDDI	IO +3.3V power supply
6	T_ACK	out		B4CR	test acknowledge
7	open				
8	open				
9	T_REQB	in		IBUFDQ	test request signal
10	T_REQA	in		IBUFDQ	test request signal
11	TROM	in		SCHMITC	boot from test Rom select
12	PA[1]	inout	inout	BD4CR	port A bit[1]
13	PA[0]	inout	inout	BD4CR	port A bit[]
14	VSS_CORE			VSSI	CORE ground
15	VDD_CORE			VDDI	CORE +3.3V power supply
16	PA14	inout		BD4CR	download mode select (CTRL-E or UART1)
17	PA15	inout		BD4CR	download mode select (UART baudrate)
18	E_CLK	inout	inout	BD8CR	EBI clock
19	open				
20	open				
21	S_nWE	out		B8CR	control signal SDRAM
22	S_nRAS	out		B8CR	control signal SDRAM
23	VSS_IO			VSSI	IO ground
24	VDD_IO			VDDI	IO +3.3V power supply
25	S_nCAS	out		B8CR	control signal SDRAM
26	S_nLDQM	out		B8CR	control signal SDRAM
27	S_nUDQM	out		B8CR	control signal SDRAM
28	E_A[15]	inout		BD8CR	adress bus / testbus MSB
29	E_A[14]	inout		BD8CR	adress bus / testbus MSB
30	VSS_IO			VSSI	IO ground
31	VDD_IO			VDDI	IO +3.3V power supply
32	open				
33	open				
34	E_A[13]	inout		BD8CR	adress bus / testbus MSB
35	E_A[12]	inout		BD8CR	adress bus / testbus MSB
36	E_A[11]	inout		BD8CR	adress bus / testbus MSB
37	E_A[10]	inout		BD8CR	adress bus / testbus MSB
38	E_A[9]	inout		BD8CR	adress bus / testbus MSB
39	VSS_CORE			VSSI	CORE ground
40	VDD_CORE			VDDI	CORE +3.3V power supply
41	E_A[8]	inout		BD8CR	adress bus / testbus MSB
42	E_A[7]	inout		BD8CR	adress bus / testbus MSB
43	E_A[6]	inout		BD8CR	adress bus / testbus MSB
44	E_A[5]	inout		BD8CR	adress bus / testbus MSB
45	E_A[4]	inout		BD8CR	adress bus / testbus MSB
46	open				
47	open				
48	VSS_IO			VSSI	IO ground
49	VDD_IO			VDDI	IO +3.3V power supply
50	E_A[3]	inout		BD8CR	adress bus / testbus MSB
51	E_A[2]	inout		BD8CR	adress bus / testbus MSB

NO.	Pin Name	Dir funct	Dir test	pad type	Description
52	E_A[1]	inout		BD8CR	adress bus / testbus MSB
53	E_A[0]	inout		BD8CR	adress bus / testbus MSB
54	E_D[0]	inout		BD8SCRDQ	data bus / testbus LSB
55	E_D[1]	inout		BD8SCRDQ	data bus / testbus LSB
56	VSS_IO			VSSI	IO ground
57	VDD_IO			VDDI	IO +3.3V power supply
58	E_D[2]	inout		BD8SCRDQ	data bus / testbus LSB
59	E_D[3]	inout		BD8SCRDQ	data bus / testbus LSB
60	E_D[4]	inout		BD8SCRDQ	data bus / testbus LSB
61	E_D[5]	inout		BD8SCRDQ	data bus / testbus LSB
62	E_D[6]	inout		BD8SCRDQ	data bus / testbus LSB
63	VSS_CORE			VSSI	CORE ground
64	VDD_CORE			VDDI	CORE +3.3V power supply
65	open				
66	open				
67	E_D[7]	inout		BD8SCRDQ	data bus / testbus LSB
68	E_D[8]	inout		BD8SCRDQ	data bus / testbus LSB
69	E_D[9]	inout		BD8SCRDQ	data bus / testbus LSB
70	E_D[10]	inout		BD8SCRDQ	data bus / testbus LSB
71	E_D[11]	inout		BD8SCRDQ	data bus / testbus LSB
72	VSS_IO			VSSI	IO ground
73	VDD_IO			VDDI	IO +3.3V power supply
74	E_D[12]	inout		BD8SCRDQ	data bus / testbus LSB
75	E_D[13]	inout		BD8SCRDQ	data bus / testbus LSB
76	E_D[14]	inout		BD8SCRDQ	data bus / testbus LSB
77	E_D[15]	inout		BD8SCRDQ	data bus / testbus LSB
78	open				
79	open				
80	S_nOE	out		B8CR	output enable
81	S_CS	out		B8CR	chip select signal (SDRAM)
82	VSS_IO			VSSI	IO ground
83	VDD_IO			VDDI	IO +3.3V power supply
84	AFTXD[3]	out		B8	transmit data nibble
85	AFTXD[2]	out		B8	transmit data nibble
86	AFTXD[1]	out		B8	transmit data nibble
87	AFTXD[0]	out		B8	transmit data nibble
88	IDDq_Sachem				
89	VSS_CORE			VSSI	CORE ground
90	VDD_CORE			VDDI	CORE +3.3V power supply
91	open				
92	CTRLDATA	inout		BD4CR	serial data transmit channel
93	MCLK	in		SCHMITC	master clock
94	CLWD	in		IBUF	start of word indication
95	AFRXD[3]	in		IBUF	receive data nibble
96	AFRXD[2]	in		IBUF	receive data nibble
97	U_TxADDR[1]				
98	VSS_IO			VSSI	IO ground
99	VDD_IO			VDDI	IO +3.3V power supply
100	U_TxADDR[3]				
101	U_TxADDR[4]				
102	AFRXD[1]	in		IBUF	receive data nibble
103	AFRXD[0]	in		IBUF	receive data nibble
104	POWER_LOWB	inout		BD4CR	Power down analog front end

NO.	Pin Name	Dir funct	Dir test	pad type	Description
105	U_TxADDR[0]	in		IBUFDQ	utopia tx adress bit
106	U_TxData[0]	in		IBUF	utopia tx data bus
107	U_TxData[1]	in		IBUF	utopia tx data bus
108	VSS_IO			VSSI	IO ground
109	VDD_IO			VDDI	IO +3.3V power supply
110	U_TxADDR[2]				
111	open				
112	U_TxData[2]	in		IBUF	utopia tx data bus
113	U_TxData[3]	in		IBUF	utopia tx data bus
114	U_TxData[4]	in		IBUF	utopia tx data bus
115	U_TxData[5]	in		IBUF	utopia tx data bus
116	U_TxData[6]	in		IBUF	utopia tx data bus
117	VSS_CORE			VSSI	CORE ground
118	VDD_CORE			VDDI	CORE +3.3V power supply
119	U_TxData[7]	in		IBUF	utopia tx data bus
120	U_TxENBB	in		IBUF	Utopia Tx enable
121	U_TxCLAV	inout		BD8SCR	Utopia Tx cell available
122	U_TxSOC	in		IBUF	transmit interface start of cell indication
123	U_TxCLK	in		IBUF	transmit interface utopia clock
124	VSS_IO			VSSI	IO ground
125	VDD_IO			VDDI	IO +3.3V power supply
126	U_RxENBB	in		IBUF	Utopia Rx enable
127	U_RxCLAV	inout		BD8SCR	Utopia Rx cell available
128	U_RxSOC	inout		BD8SCR	receive interface start of cell indication
129	U_RxCLK	in		IBUF	receive interface utopia clock
130	U_TxRefB	in		IBUFDQ	8 kHz clock from network
131	U_RxRefB	inout		BD4CR	8 kHz clock to ATM device
132	open				
133	U_RxADDR[1]				
134	VSS_IO			VSSI	IO ground
135	VDD_IO			VDDI	IO +3.3V power supply
136	U_RxADDR[3]				
137	U_RxADDR[4]				
138	U_RxADDR[0]	in		IBUFDQ	Utopia rx adress bit
139	U_RxData[7]	outZ		BD8SCR	Utopia rx data bus
140	U_RxData[6]	outZ		BD8SCR	Utopia rx data bus
141	U_RxData[5]	outZ		BD8SCR	Utopia rx data bus
142	U_RxData[4]	outZ		BD8SCR	Utopia rx data bus
143	VSS_CORE			VSSI	CORE ground
144	VDD_CORE			VDDI	CORE +3.3V power supply
145	U_RxADDR[2]				
146	U_RxData[3]	outZ		BD8SCR	Utopia rx data bus
147	U_RxData[2]	outZ		BD8SCR	Utopia rx data bus
148	U_RxData[1]	outZ		BD8SCR	Utopia rx data bus
149	U_RxData[0]	outZ		BD8SCR	Utopia rx data bus
150	open				
151	SACHEM_RESETB	in		IBUF	sachem hard reset, active low
152	VSS_IO			VSSI	IO ground
153	VDD_IO			VDDI	IO +3.3V power supply
154	C_A[8]	inout	inout	BD8CR	Ctrl_E adress bus
155	C_A[7]	inout	inout	BD8CR	Ctrl_E adress bus
156	C_A[6]	inout	inout	BD8CR	Ctrl_E adress bus
157	C_A[5]	inout	inout	BD8CR	Ctrl_E adress bus

NO.	Pin Name	Dir funct	Dir test	pad type	Description
158	C_A[4]	inout	inout	BD8CR	Ctrl_E adress bus
159	C_A[3]	inout	inout	BD8CR	Ctrl_E adress bus
160	VSS_IO			VSSI	IO ground
161	VDD_IO			VDDI	IO +3.3V power supply
162	open				
163	open				
164	C_A[2]	inout	inout	BD8CR	Ctrl_E adress bus
165	C_A[1]	inout		BD8CR	Ctrl_E adress bus
166	C_A[0]	inout		BD8CR	Ctrl_E adress bus
167	C_D[7]	inout	inout	BD8CR	Ctrl_E data bus
168	C_D[6]	inout	inout	BD8CR	Ctrl_E data bus
169	VSS_CORE			VSSI	CORE ground
170	VDD_CORE			VDDI	CORE +3.3V power supply
171	C_D[5]	inout	inout	BD8CR	Ctrl_E data bus
172	C_D[4]	inout	inout	BD8CR	Ctrl_E data bus
173	C_D[3]	inout	inout	BD8CR	Ctrl_E data bus
174	C_D[2]	inout		BD8CR	Ctrl_E data bus
175	C_D[1]	inout		BD8CR	Ctrl_E data bus
176	open				
177	open				
178	VSS_IO			VSSI	IO ground
179	VDD_IO			VDDI	IO +3.3V power supply
180	C_D[0]	inout		BD8CR	Ctrl_E data bus
181	C_clk	in		SCHMITC	Ctrl_E serial input clock
182	C_notCS	in		SCHMITC	Ctrl_E chip select
183	C_notWr	in		SCHMITC	Ctrl_E write indication
184	C_notRd	inout		BD4CR	Ctrl_E read indication
185	C_mode[1]				
186	VSS_IO			VSSI	IO ground
187	VDD_IO			VDDI	IO +3.3V power supply
188	C_notRdy	out_Hiz		BT4CR	Ctrl_E ready indication
189	open				
190	C_notInt	out_Hiz		BT4CR	Ctrl_E interface interrupt
191	MODE[1]	in		IBUF	select functionnal and test mode
192	MODE[0]	in		IBUF	select functionnal and test mode
193	SCAN_CLK	in		SCHMITC	scan clock
194	VSS_CORE			VSSI	CORE ground
195	VDD_CORE			VDDI	CORE +3.3V power supply
196	TESTSE	in	in	SCHMITCDQ	test scan enable
197	RSRXD1	inout		BD4CR	serial Rx port
198	RSTXD1	inout		BD4CR	serial Tx port
199	open				
200	open				
201	C_mode[0]	in		SCHMITCDQ	Ctrl-E mode signal : =motorola, 1=intel
202	IDDq_CARM				
203	TCK	in	in	IBUFUQ	jtag clock
204	VSS_IO			VSSI	IO ground
205	VDD_IO			VDDI	IO +3.3V power supply
206	nTRST	in	in	IBUFDQ	reset jtag interface
207	TMS	in	in	IBUFUQ	test mode select
208	TDO	out	out	BT4CR	test data out

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